Sierra Components, Inc.

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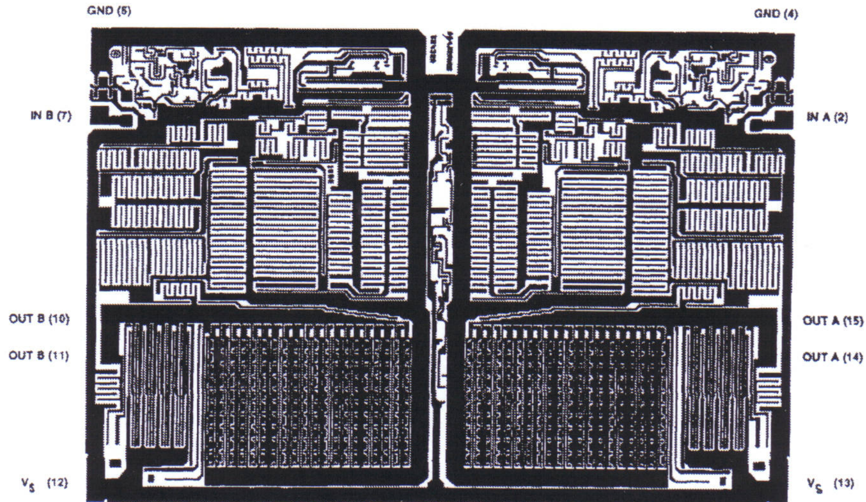
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

Die physical dimensions.
- Die size: 3370 microns x 4890 microns.
- Die thickness: 19 ± 1 mils.

Interface materials.
- Top metallization: Al Si Cu 16.0 kÅ ±2 kÅ
- Backside metallization: None

Glassivation.
- Type: PSG
- Thickness: 8.0 kÅ ±1.0 kÅ

Substrate: DI (dielectric isolation)

Assembly related information.
- Substrate potential: Unbiased
- Special assembly instructions: None

FIGURE A-1. Die bonding pad locations and electrical functions.

Top Material:Al, Si, Cu
Backside Material: Si
Bond Pad Size:
Backside Potential:
Mask Ref:

APPROVED BY:RB	DIE SIZE :3370 x 4890mic	DATE: 9/1/09
MFG:Intersil	THICKNESS:	P/N:HS4424B